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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CHOW, CHARLES CHIANG	
ART UNIT	**PAPER NUMBER**
2685	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/617,485	JAEHNE ET AL.	
	Examiner	Art Unit	
	Charles Chow	2685	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:
A person shall be entitled to a patent unless –

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1-5, 9, 12, 15-21, 23, 26 are rejected under 35 U.S.C. 102(e) as being anticipated by Olgaard (US 6,236,278 B1).

Regarding **claim 1.** Olgaard has taught a phase locked loop PLL device [Fig. 6A] which comprises a prescaler [665] for dividing the frequency of an output signal of the phase locked loop device by a prescaler factor [dividing Fout from vco 640 by N, N+1, col. 7, lines 45-48],

said prescaler 665 being operable in at least two modes, each mode having assigned a different prescaler factor [the prescaler 665 has two dividing modes, one mode is to divide frequency by a prescaler factor of value N, & other mode is to divide by a value of N+1, col. 7, lines 45-48 & col. 8, lines 31-39]; and

there is an accumulator [670] connected to said prescaler 665 for providing a mode switching signal [the accumulator 670 & MOD 671 provides the mode switching signal 654, col. 7, line 43 to col. 8, line 67] to said prescaler [665], said accumulator 670 storing an accumulator value [the accumulator 670 stores the tune numerator value from 675 & modulus demominator value from 676 to B of 671, col. 8, lines 5-15].

wherein said accumulator 670 is adapted to repetitively update said accumulator value using a modulus function 671, to generate said mode switching signal 654 [the accumulator

670 repetitively updates the accumulated value via the feedback at input B from modulus 671, col. 8, lines 20-31; to generate mode switching signal 654 via overflow OVF 672 from modulus 671 & 654 from cycle slip 652, col. 8, lines 20-67 & table 1, table 2.].

Regarding **claim 2**. Olgaard teaches the PLL device [Fig. 6A] wherein said accumulator [670] is connected to receive a tune parameter [675] selected for tuning the frequency of said output signal [to tune fout into fractional frequency having denominator value in 676],

wherein said accumulator [670] is adapted to take into account said tune parameter [taking into account at A input of 670 of the tune value from numerator 675], when processing the modulus function for generating said mode switching signal [the processing modulus function at modulus 671 using modulus value from denominator 676 to be load at B input of 671, to generate 654 via OVF 672, col. 8, lines 20-67, table 1, table 2].

Regarding **claim 3.** Olgaard teaches the PLL device [Fig. 6A] comprising a divider unit [650] connected to said prescaler [665] for dividing the frequency of the prescaler output by a fixed divider factor [divide by B value],

wherein said accumulator [670] is adapted for processing said modulus function dependent on a received modulus parameter [the modulus parameter is loaded to B input of 671 from denominator register 676, to perform (ACCU output) MOD by (DENOM) in 671, col. 8, lines 15-32, table 1, table 2] , and said fixed divider factor [divide by B value] is equal to said modulus parameter [the modulus value from denominator 676 at terminal B].

Regarding **claim 4.** Olgaard teaches the PLL device [Fig. 6A] wherein said accumulator [670] is adapted for taking into account a modulus parameter [the modulus value from denominator 676 at terminal B] and receiving a tune parameter [the tune numerator value from 675 at A input of 670],

the modulus parameter [B input of 671] being a fixed divider factor of a divider unit

[the divide value B at 605] of the phase locked loop device, the tune parameter [675] being selected for tuning the frequency of said output signal [to tune fout into fractional frequency having denominator value in 676]

wherein said accumulator [670] is adapted to take into account said modulus parameter and said tune parameter [the taking into account of modulus parameter at B input of 671 and tune parameter at A input of 670] when processing the modulus function for generating said mode switching signal [the processing modulus function at modulus 671 using modulus value from denominator 676 to be load at B input of 671, to generate 654 via OVF 672, col. 8, lines 20-67, table 1, table 2].

Regarding **claim 5.** Olgaard teaches the PLL device [Fig. 6A] wherein said accumulator [670] is adapted to calculate the sum of the accumulator value and the tune parameter and to calculate the accumulator value to be the result of applying said modulus function to said sum and said modulus parameter [col. 8, lines 20-45, (ACCU output) MOD by (DENOM) in table 1, table 2].

Regarding **claims 9, 23,** Olgaard teaches the PLL device [Fig. 6A] further comprising an input terminal [f_{REF} input to 610] for receiving a reference signal having a frequency [f1] to be compared with a frequency [f2] of a phase locked loop feedback signal for adjusting the frequency of said output signal [to adjusting f_{OUT} via the phase locked loop operation].

Regarding **claims 12, 26,** Olgaard teaches the PLL device [Fig. 6A] adapted for being operated as a frequency synthesizer [col. 4, lines 64-66].

Regarding **claim 15.** Olgaard teaches a method of operating a phase locked loop device col. 5, lines 54-57 & Fig. 6A], the method comprising dividing the frequency of an output signal [f_{OUT}] of the phase locked loop device in a prescaler [665] of said phase locked loop device by a prescaler factor [N/ N+1 or K/K+1], said prescaler [665] being operable in at

least two modes, each mode having assigned a different prescaler factor [one mode to divide by N, other mode to divide by N+1, col. 7, liens 43-48]; and generating a mode switching signal [654 via OVF 672] for changing the mode of said prescaler [665],

wherein generating the mode switching signal comprises storing an accumulator value; and processing a modulus function for updating said accumulator value [col. 8, lines 20-45].

Regarding **claim 16.** Olgaard teaches the PLL device [Fig. 6A] wherein the step of processing said modulus function [671, (ACCU) MOD (DENOm) in table 1 & 2] comprises receiving a tune parameter for tuning the frequency of said output signal [the receiving . tune numerator 675, to tune fout into fractional frequency, having denominator value in 676].

Regarding **claim 17.** Olgaard teaches the PLL device [Fig. 6A] wherein the step of dividing the frequency of said output signal comprises dividing the frequency of a prescaler output by a fixed divider factor [the divide by B fixed value at 650];

wherein processing said modulus function [671] depends on a received modulus parameter [modulus input at B input of 671], wherein said fixed divider factor [B in 650] is equal to said modulus parameter [the modulus value input to B input of 671; the (ACCU) MOD (DENOM) in table 1 & 2, col. 8, lines 24].

Regarding **claim 18.** Olgaard teaches the PLL device [Fig. 6A] wherein the step of processing said modulus function [col. 20, lines 30-50] comprises receiving a modulus parameter [denominator 676 at B input of 671] and a tune parameter [numerator value 675 at A input of 670],

said modulus parameter [676] being a fixed divider factor [B] and said tune parameter being selected for tuning the frequency of said output signal [the numerator 675 for tuning the fractional output frequency] , and

taking into account said modulus parameter and said tune parameter when updating said accumulator value [col. 8, lines 20-45].

Regarding **claim 19.** Olgaard teaches the wherein the step of processing said modulus function [method in col. 18, line 41 & table 1 & 2] further comprises calculating a sum of said accumulator value and said tune parameter, and calculating said updated accumulator value to be the result of applying said modulus function to said sum and said modulus parameter [the adding of updated MOD feedback at B input of 670 to A input of 670, to update the accumulator, updated at the end of each system cycle, col. 8, lines 20-45].

Regarding **claim 20.** Olgaard teaches the PLL device [Fig. 6A] wherein the step of calculating [method in col. 18, line 41, table 1 & 2] further comprises storing said sum as the updated accumulator value in a register [the storing the updated accumulator value with the summation of the updated MOD feedback at B input of 670 to the value at A of 670, for every end of system cycle, col. 8, lines 20-45].

Regarding **claim 21.** Olgaard teaches the PLL device [Fig. 6A] wherein the step of calculating said sum [method in col. 18, line 41, table 1 & 2] comprises subtracting said modulus parameter from said sum [the modulus function performed by 671 is to subtraction modulus parameter from sum, resulting with the remainder 2, 4 in, 0r2, 0r4 of in table 1 & 2], and storing the difference as the updated accumulator value in a register [the storing updated MOD result, remainder 2, 4, back to B input of accumulator 670] .

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject

matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Olgaard in view of Han et al. (US 2003/0108,143 A1).

Regarding **claim 6,** olgaard fails to teach the hard coded modulus parameter which is taught by Han et al. (Han) [the hard coded 3-bit width delta-sigma modulator in Fig. 6, 41 in Fig. 7 for providing modulus control to prescaler 31 in Fig. 7, paragraph 0061-0068], to reduce the spurious noise signal [0079]. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify Olgaard with the teachings from Han's 3-bit modulus controlling for prescaler, in order to modulate the prescaler to reduce the spurious noise signal.

3. Claims 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Olgaard in view of Humphreys et al. (US 2002/0198,912 A1).

Regarding **claim 7,** Olgaar fails to teach the wherein said accumulator comprises a plurality of subunits having reduced bit widths. Humphreys et al. (Humphreys) teaches these features [the accumulator 210 is divided into three cascaded sections, 225-1/230-1 to 225-3/230-3, to produce dividing sequences from 3 carry outputs C01 to C03, Fig. 2, paragraphs 0016-0019 & 0042; each section has a 3-bit structure in Fig. 4; 3-bit bus & n=C=3 in paragraph 0032-0033; paragraphs 0031-0039], in order to flexibly vary the fractional denominator D for each cascaded section [0020-0022]. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify Olgaard with the teachings from Humphreys' cascaded 3-bit in accumulator 210, in order to upgrade the PLL with flexibly denominator D in each 3-bit section in the accumulator.

Regarding **claim 8,** in combination, Humphreys teaches the wherein the 3-bit width of each subunit 225/230 of said accumulator 210 is three bits [Fig. 4, paragraphs 0016-0019, 0042 & 0031-0039].

4. Claims 11, 14, 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Olgaard in view of Lee (US 2002/0025,778 A1).

Regarding **claims 11, 25,** olgaard fails to teach the features for this claim. Lee teaches the PLL device adapted for being operated in a transceiver of a WLAN (Wireless Local Area Network) communication system [PLL 250 in Fig. 5, paragraphs 0041, 0044], in order to enable user to tune to WLAN frequency using PLL 250 for transceiver. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify Olgaard with the teachings from Lee's PLL 250 for WLAN system.

Regarding **claim 14.** Olgaard teaches a PLL device [Fig. 6A] comprising a prescaler 665 for dividing the frequency of an output signal f_{OUT} of the phase locked loop device by a prescaler factor [N/N+1 or K/K+1, Fig. 6A],

said prescaler 665 being operable in at least two modes, each mode having assigned a different prescaler factor [the prescaler 665 has two dividing modes, one mode is to divide frequency by a prescaler factor of value N, & other mode is to divide by a value of N+1, col. 7, lines 45-48 & col. 8, lines 31-39]; and

there is an accumulator [670] connected to said prescaler 665 for providing a mode switching signal [the accumulator 670 & MOD 671 provides the mode switching signal 654; col. 7, line 43 to col. 8, line 67] to said prescaler [665], said accumulator 670 storing an accumulator value [the accumulator 670 stores the tune numerator value from 675 & modulus demominator value from 676 to B of 671, col. 8, lines 5-15].

wherein said accumulator 670 is adapted to repetitively update said accumulator value using a modulus function 671, to generate said mode switching signal 654 [the accumulator 670 repetitively updates the accumulated value via the feedback at input B from modulus 671, col. 8, lines 20-31; to generate mode switching signal 654 via overflow OVF 672 from modulus 671 & 654 from cycle slip 652, col. 8, lines 20-67 & table 1, table 2.].

Olgaard fails to teach a PLL device for a transceiver in a WLAN communication system. Lee teaches these features [PLL 250 in Fig. 5, paragraphs 0041, 0044], in order to enable user to tune to WLAN frequency using PLL 250 for transceiver. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify Olgaard with the teachings from Lee's PLL 250 for WLAN system.

5. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Olgaard in view of Harpham (US 2001/0017,572 A1).

Regarding **claim 13,** Olgaard teaches a PLL device [Fig. 6A] comprising a prescaler 665 for dividing the frequency of an output signal f_{OUT} of the phase locked loop device by a prescaler factor [N/N+1 or K/K+1, Fig. 6A],

said prescaler 665 being operable in at least two modes, each mode having assigned a different prescaler factor [the prescaler 665 has two dividing modes, one mode is to divide frequency by a prescaler factor of value N, & other mode is to divide by a value of N+1, col. 7, lines 45-48 & col. 8, lines 31-39]; and

there is an accumulator [670] connected to said prescaler 665 for providing a mode switching signal [the accumulator 670 & MOD 671 provides the mode switching signal 654, col. 7, line 43 to col. 8, line 67] to said prescaler [665].

Olgaard fails to teach the integrated circuit IC chip having a phase locked loop PLL circuit. Harpham teaches these features [the IC chip 13 for a PLL in Fig. 2, with accumulators 31-32, paragraphs 0026, 0043, 0054], to reduce the size of PLL for an IC Chip. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify Olgaard with the teachings from Harpham's IC chip PLL 13, in order to reduce the size of a PLL for IC chip.

6. Claims 10, 24, are rejected under 35 U.S.C. 103(a) as being unpatentable over Olgaard in view of Takeuchi (US 5,521,948).

Regarding **claims 10, 24,** Olgaard fails to teach the changing said mode switching for at least three times in each period of frequency signal.

Takeuchi teaches these features, in his method steps, & the wherein said accumulator, is adapted for changing said mode switching signal at least three times in each period of said reference signal [the control unit 30 in Fig. 5 produces at least three mode switching signal per reference signal period t12 to t13 or t13 to t14, for switching modulus dividing values in between N, N+1 in prescalers 26-29, Fig. 6A-6E, col. 6, lines 20-50], to immediately correct the phase error [col. 2, lines 49-63]. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify Olgaard with the teachings from Takeuchi's multiple dividing mode switching per period of the reference signal, in order to immediately correct the phase error.

7. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Olgaard in view of Kasturia (US 5,572,168).

Regarding **claim 22,** Olgaard teaches the comparing the accumulator's sum [the monitoring of the modulus operation at 680 by comparing the output from 671 with the input at B from 685, col. 10, lines 59-67], but olgaard fails to teach the other claim limitations.

Kasturia teaches the wherein further comprising comparing remaining counts in swallow counter 24 with said modulus parameter [the comparing of the modulus parameters D1 to D7 with the content of the swallow counter 24 in Fig. 5, to generate modulus dividing control] & to calculating the updated accumulated count value comprises changing the mode switching signal such that said prescaler 22 changes its mode depending on the comparing result [col. 4, line 56 to col. 5, line 10, Fig.5], in order to suppression the phase error [col. 2, lines 27-33]. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify Olgaard with the teachings from Kastria's comparing the count value with the modulus value D1-D7, in order to suppression the phase error.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles Chow whose telephone number is (571) 272-7889. The examiner can normally be reached on 8:00am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Urban can be reached on (571) 272-7899. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Charles Chow C.C.

January 6, 2006.

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